Amendments to the Claims:

Please amend claims 43, 48, 51, 52, 55 and 56 as shown in the listing of claims below. This listing of claims will replace all prior versions and listings of claims in the application:

1-42. (canceled)

43. (currently amended) A timing recovery system for generating a set of clock signals in a processing system, the set of clock signals comprising a set of sampling clock signals associated with a corresponding plurality of input signals, the processing system comprising a set of processing subsystems, each of the processing subsystems comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, the timing recovery system ~~comprsing~~ comprising:

(a) a set of phase detectors generating phase errors for the corresponding sampling clock signals;

(b) a set of loop filters coupled to the corresponding phase detectors, the loop filters receiving the corresponding phase errors and generating filtered phase errors;

(c) a set of digital-to-analog (D/A) converters coupled to the loop filters, the D/A converters receiving the filtered phase errors and generating analog filtered phase errors; and

(d) a set of oscillators coupled to the corresponding D/A converters, the oscillators receiving the analog filtered phase errors and generating the sampling clock signals, wherein the sampling clock signals so generated are transmitted to respective subsystems;

wherein the set of clock signals further comprises a receive clock signal and wherein each of the processing subsystems further comprises a digital section, the digital sections operating in accordance with the received clock signal.

44. (previously presented) The timing recovery system of claim 43 wherein the receive clock signal is related to one of the sampling clock signals.

45. (previously presented) The timing recovery system of claim 44 further comprising a first adder and a receive clock phase selector, the first adder receiving one of the phase control signals and a receive clock offset and generating a phase shift value, the receive clock phase selector receiving the phase shift value and generating the receive clock signal.

46. (previously presented) The timing recovery system of claim 45 wherein the phase shift value comprises a set of phase steps and wherein the receive clock phase selector receives the phase shift value in the form of consecutive phase steps.

47. (canceled)

48. (currently amended) A timing recovery system for generating a set of clock signals in a processing system, the set of clock signals comprising a transmit clock signal and a set of sampling clock signals associated with a corresponding plurality of input signals, the processing system comprising a set of processing subsystems, each of the processing subsystems comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, each of the processing subsystems further comprising a transmit section, the transmit sections operating in accordance with the transmit clock signal, the timing recovery system ~~comprsing~~ comprising:

(a) a set of phase detectors generating phase errors for the corresponding sampling clock signals;

(b) a set of loop filters coupled to the corresponding phase detectors, the loop filters receiving the corresponding phase errors and generating filtered phase errors;

(c) a set of digital-to-analog (D/A) converters coupled to the loop filters, the D/A converters receiving the filtered phase errors and generating analog filtered phase errors; and

(d) a set of oscillators coupled to the corresponding D/A converters, the oscillators receiving the analog filtered phase errors and generating the sampling clock

signals, wherein the sampling clock signals so generated are transmitted to respective subsystems; and

a transmit clock phase selector, the transmit clock phase selector receiving a transmit clock offset and generating the transmit clock signal.

49. (previously presented) The timing recovery system of claim 48 wherein the transmit clock offset is equal to zero.

50. (canceled)

51. (currently amended) A timing recovery system for generating a set of clock signals in a processing system, the set of clock signals comprising a transmit clock signal and a set of sampling clock signals associated with a corresponding plurality of input signals, wherein the transmit clock signal is related to one of the sampling clock signals, the processing system comprising a set of processing subsystems, each of the processing subsystems comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, each of the processing subsystems further comprising a transmit section, the transmit sections operating in accordance with the transmit clock signal, the timing recovery system ~~comprsing~~ comprising:

(a) a set of phase detectors generating phase errors for the corresponding sampling clock signals;

(b) a set of loop filters coupled to the corresponding phase detectors, the loop filters receiving the corresponding phase errors and generating filtered phase errors;

(c) a set of digital-to-analog (D/A) converters coupled to the loop filters, the D/A converters receiving the filtered phase errors and generating analog filtered phase errors; and

(d) a set of oscillators coupled to the corresponding D/A converters, the oscillators receiving the analog filtered phase errors and generating the sampling clock signals, wherein the sampling clock signals so generated are transmitted to respective subsystems; and

a transmit clock phase selector, the transmit clock phase selector receiving a phase control signal and generating the transmit clock signal.

52. (currently amended) A timing recovery system for generating a set of clock signals in a processing system, the set of clock signals comprising a set of sampling clock signals associated with a corresponding plurality of input signals, the processing system comprising a set of processing subsystems, each of the processing subsystems comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, the timing recovery system ~~comprsing~~ comprising:

(a) a set of phase detectors generating phase errors for the corresponding sampling clock signals, wherein each of the phase detectors receives a corresponding slicer error and a corresponding tentative decision from a decoding system;

(b) a set of loop filters coupled to the corresponding phase detectors, the loop filters receiving the corresponding phase errors and generating filtered phase errors;

(c) a set of digital-to-analog (D/A) converters coupled to the loop filters, the D/A converters receiving the filtered phase errors and generating analog filtered phase errors; and

(d) a set of oscillators coupled to the corresponding D/A converters, the oscillators receiving the analog filtered phase errors and generating the sampling clock signals, wherein the sampling clock signals so generated are transmitted to respective subsystems.

53. (previously presented) The timing recovery system of claim 52 wherein each of the phase detectors comprises a lattice structure, the lattice structure comprising two delay elements, two multipliers and an adder, the lattice structure generating a pre-cursor phase error by multiplying the corresponding tentative decision by a delayed version of the corresponding slicer error and generating a post-cursor phase error by multiplying the corresponding slicer error by a delayed version of the corresponding tentative decision and

combining the pre-cursor and post-cursor phase errors to produce the corresponding phase error.

54. (previously presented) The timing recovery system of claim 53 wherein at least one of the phase detectors further receives an offset input from a control unit and wherein the associated lattice structure combines the pre-cursor, post-cursor phase errors and the offset input to produce the corresponding phase error.

55. (currently amended) A timing recovery system for generating a set of clock signals in a processing system, the set of clock signals comprising a set of sampling clock signals associated with a corresponding plurality of input signals, the processing system comprising a set of processing subsystems, each of the processing subsystems comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, the timing recovery system ~~comprsing~~ comprising:

(a) a set of phase detectors generating phase errors for the corresponding sampling clock signals;

(b) a set of loop filters coupled to the corresponding phase detectors, the loop filters receiving the corresponding phase errors and generating filtered phase errors, wherein at least one of the loop filters comprises a first filter for accumulating a number of consecutive values of one of the phase errors to produce a filtered phase error;

(c) a set of digital-to-analog (D/A) converters coupled to the loop filters, the D/A converters receiving the filtered phase errors and generating analog filtered phase errors; and

(d) a set of oscillators coupled to the corresponding D/A converters, the oscillators receiving the analog filtered phase errors and generating the sampling clock signals, wherein the sampling clock signals so generated are transmitted to respective subsystems.

56. (currently amended) A timing recovery system for generating a set of clock signals in a processing system, the set of clock signals comprising a set of sampling clock signals

associated with a corresponding plurality of input signals, the processing system comprising a set of processing subsystems, each of the processing subsystems comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, the timing recovery system ~~comprsing~~ comprising:

(a) a set of phase detectors generating phase errors for the corresponding sampling clock signals;

(b) a set of loop filters coupled to the corresponding phase detectors, the loop filters receiving the corresponding phase errors and generating filtered phase errors, wherein at least one of the loop filters comprises a first filter for accumulating a number of consecutive values of one of the phase errors to produce a sum value, and a second filter for integrating the sum value to produce an integral value and an adder for combining the sum value and the integral value to produce a filtered phase error;

(c) a set of digital-to-analog (D/A) converters coupled to the loop filters, the D/A converters receiving the filtered phase errors and generating analog filtered phase errors; and

(d) a set of oscillators coupled to the corresponding D/A converters, the oscillators receiving the analog filtered phase errors and generating the sampling clock signals, wherein the sampling clock signals so generated are transmitted to respective subsystems.

57. (previously presented) The timing recovery system of claim 56 wherein the second filter includes a multiplier for scaling the integrated sum value by a scale factor to produce the integral value.

58-60. (canceled)